Amendments to the Drawings:

The attached four (4) sheets of drawings include changes to Figs. 2C, 4A, 4B, and 4C. In Fig. 2C, the time indicators "0.0" and "$-1.0X10^{-5}$" along the time axis are changed to --$9.0X10^{-4}$-- and --$8.0X10^{-4}$--, respectively. In Figs. 4A, 4B, and 4C, the reference characters not mentioned in the specification have been deleted. These sheets, which include Figs. 2C, 4A, 4B, and 4C, replace the original sheets that includ Figs. 2C, 4A, 4B, and 4C.

Attachment: 4 Replacement Sheets
4 Annotated Sheets Showing Changes

REMARKS/ARGUMENTS

Claims 1-31 are pending. Claims 1-13 and 21-31 were previously withdrawn from consideration pursuant to a restriction requirement. No claim amendments are made herein.

Office Action summary

Figs. 3, 4A, 4B and 4C were objected for including reference characters not mentioned in the specification.

Claims 14 and 16-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (APA) in view of US Patent No. 6,469,344 to Iwamuro et al. (Iwamuro). Claim 15 was rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Iwamuro, US Patent No. 5,793,064 to Li (Li), and US Patent No. 4,987,098 to Nishiura et al. (Nishiura). Claim 19 was rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Iwamuro and US Patent No. 5,008,720 to Uenishi (Uenishi). Claim 20 was rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Iwamuro and European Patent Application No. EP 1193767 to Matsudai et al (Matsudai).

Specification amendment

Paragraph [0041] is amended to correct an inadvertent error, namely, "a second pn junction 321" is changed to --a second pn junction 323--. This amendment brings the specification into conformity with Fig. 3.

Paragraph [0045] is amended to bring it into conformity with what is shown in Figs. 4A-4C. Namely, "as shown in Figs. 4A through 4C, hole current is uniformly distributed" is changed to --as shown in Figs. 4A through 4C, a substantially similar pattern of hole current distribution can be observed--.

No new matter is believed added.

Objections to the drawings

Fig. 3 is objected for including a reference numeral that is not mentioned in the specification. It is believed the above amendment to paragraph [0041] of the specification addresses this objection.

Figs. 4A, 4B, and 4C are objected to for including reference characters not mentioned in the specification. As shown in the attached amended drawings, the reference characters not mentioned in the specification have been removed from Figs. 4A, 4B, and 4C.

Fig. 2C has also been amended to correct inadvertent errors, namely, the time indicators "0.0" and "$-1.0X10^{-5}$" along the time axis have been changed to --$9.0X10^{-4}$-- and --$8.0X10^{-4}$--, respectively. This corrects what would otherwise be a nonsensical time scale.

No new matter is believed added.

Rejection of Claims 14-20

Claim 14 was rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Iwamuro. This is respectfully traversed.

The Examiner indicates that the APA fails to teach or suggest a floating second well region as recited in applicants' claim 14, and then attempts to overcome this deficiency by combining what the Examiner terms as the "well region floating (5)" in Fig. 1 of Iwamauro with prior art Fig. 2A of the present application. The Examiner then states:

> "It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of APA to include a second well region floating as disclosed in Iwamuro because it aids in reducing on-resistance (For Example: See Abstract)."

Underline is added. This is respectfully traversed because well region 5 in Fig. 1 of Iwamuro does **not** reduce the ON resistance. Rather, well region 5 helps reduce the turn-off storage time of the device by forming p channels 17 and 18 with adjacent p well regions 4. Incorporating well region 5 in the Fig. 2A structure of APA in the manner taught by Iwamura would not yield a structure where well region 5 can form p channels with its adjacent regions as in Iwamuro, and thus the reduced turn-off storage time would not be realized. The n-type JFET

region 210 in Fig. 2A (which is doped higher than drift region 106 to reduce the device ON resistance), would further block formation of such p channels in the Fig. 2A structure. Thus, as set forth in more detail next, Iwamuro fails to provide any motivation for combining well region 5 with APA in the manner suggested by the Examiner.

According to Iwamuro, the Fig. 1 structure improves upon the prior art structure in Fig. 7. These two figures are reproduced below.

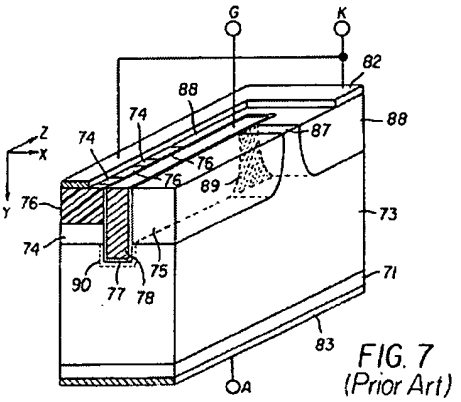


FIG. 7
(Prior Art)

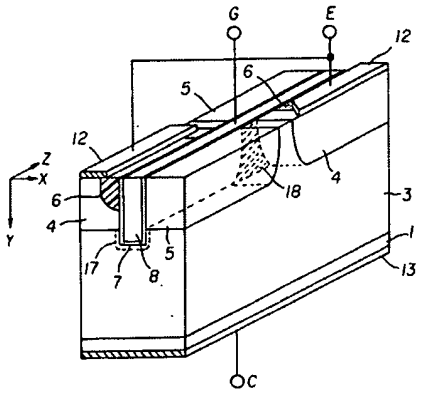


FIG. 1

In columns 2-3 of the Background section, Iwamuro describes the structure and operation of the prior art device shown in Fig. 7, and then at top of column 4 outlines the drawbacks of the Fig. 7 structure, including:

> Also, the p^+ region 88 needs to be provided for allowing carriers to be drawn away, but current does not flow through the p^+ region 88 while the device is in the ON state. Thus, the p^+ region 88 provides useless space upon turn-on, and therefore the ON-state voltage (ON resistance) of the device is increased. [Column 4, lines 6-11; underline is added]

Thus, the prior art Fig. 7 structure suffers from increased ON resistance because no current flows through p+ region 88 when the device is in the ON state. In Fig. 1, Iwamuro improves the ON resistance of the Fig. 7 structure by eliminating p+ region 88 and replacing it with well region 4 which conducts current when the device in the ON state:

> Since the p^+ region 88 provided in the trench IEGT does not perform any function while the device is in the ON state, thus providing a useless or wasteful space, the elimination of the p^+ region 88 in the present device leads to a significantly improved efficiency in utilizing the area, thus yielding such great effects as a reduction in the chip size and an increase in the current capacity. [Column 8, lines 33-39; underline is added]

That the ON resistance of the prior art structure in Fig. 7 is reduced by eliminating the p+ region is further eluded to in column 11, lines 22-26 of Iwamuro:

> [T]he first base region serves as a p^+ region that would be provided in the trench IEGT as one type of known device, thus eliminating the need to provide the p^+ region, with results of an increased effective area and reduced ON resistance.

Underlines are added. Iwamuro thus makes abundantly clear that the ON resistance of the prior art structure in Fig. 7 is improved by eliminating p^+ region 88 and replacing it with p well region 4 (Fig. 1). Therefore, it is the use of p well region 4 in place of the p^+ region 88 that improves the device ON resistance, not the presence of well region 5 as asserted by the Examiner. This is further supported by the fact that well region 5 is also present, in an identical form, in the prior art Fig. 7 structure (as well region 75).

Thus, contrary to the Examiner's assertion, one skilled in the art would not be motivated to combine well region 5 of Iwamuro with APA to improve the ON resistance of APA because Iwamura's well region 5 does not improve the ON resistance of the device. Accordingly, withdrawal of this rejection is respectfully requested.

For the reasons stated next, incorporating well region 5 in the structure shown in Fig. 2A of the present application would not reduce the turn-off storage time of the resulting structure, as it does in Fig. 1 of the Iwamura. Thus, Iwamura can not be combined with Fig. 2A of the present application for this reason either.

In Fig. 1 of Iwamuro, well region 5 is carefully integrated in the structure so that when the device is turned off, p channels 17 and 18 are formed between well region 5 and its adjacent well regions 4 (see column 7, lines 52-59). P channel 17 in Fig. 1 is formed directly underneath the gate trench and p channel 18 is formed along the trench sidewall. During turn-off

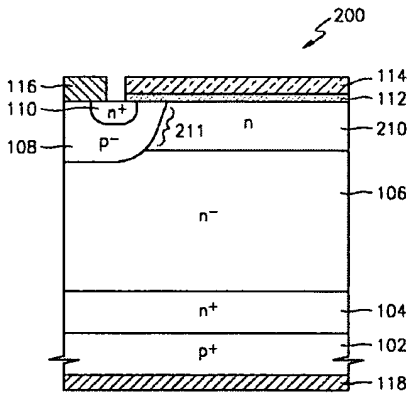
time, these two p channels provide current paths through which carriers accumulated in the vicinity of well region 5 are removed, thus reducing the device turn-off storage time:

> [T]he length of the p channel 18 is smaller than one half of that of the p channel 17. With this arrangement, a considerably large quantity of carriers that have been accumulated in the vicinity of the second p base region 5 enter the first p base region 4 through the side-wall p channel 18, to be drawn away through the emitter electrode 12, which results in a reduction in the turn-off storage time.

Thus, Iwamuro achieves a fast turn-off storage time by forming two p channels 17 and 18, one under the gate trench and one along the trench sidewall, through which accumulated carriers can be quickly removed when the device is turned off.

Applicants contend that well region 5 of Iwamuro can not be combined with the prior art structure in Fig. 2A of the present application for the purpose of obtaining a fast turn-off storage time because the two p channels required for the fast turn-off storage time would not be formed in the resulting structure. The two p channels would not be formed because of the significant structural differences between the device in Fig. 1 of Iwamuro and the prior art device in Fig. 2 of the present application. These two figures are reproduced below for comparison.

FIG. 2A



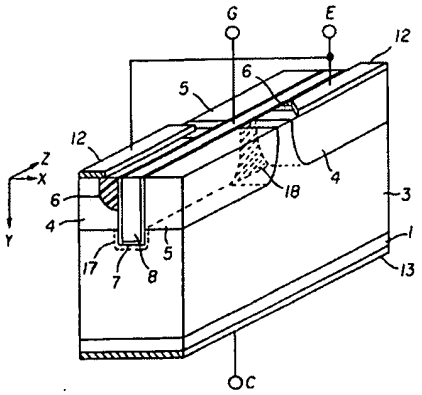


FIG. 1

As can be seen, gate 114 in Fig. 2A extends laterally over a surface of the semiconductor. In contrast, gate 8 in Fig. 1 of Iwamuro is embedded in a trench extending

vertically into the semiconductor. In Fig. 1 of Iwamuro, when the device is turned off, p channel 17 forms directly under the trench housing gate 8, and p channel 18 forms along the trench sidewall between well region 5 and well region 4. Because the structure in Fig. 2A (particularly the gate) is very different from that in Fig. 1 of Iwamuro, integrating well region 5 in Fig. 2A of the application as taught by Iwamuro would not yield a structure where p channels can form during turn-off time, and thus the reduced turn-off storage time would not be realized. Further, in Fig. 2A of the present application, n-type JFET region 210 (which is doped higher than the drift region 106 to reduce the device ON resistance) prevents formation of a p channel between p region 108 and a well region incorporated therein. To this extend, Fig. 2A teaches away from including therein well region 5 for purposes of forming p channels during turn-off time.

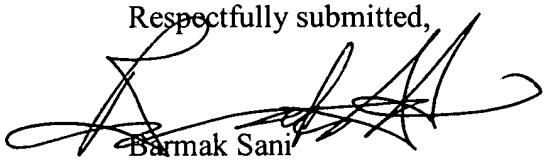
Thus, claim 14 distinguishes over Iwamuaro and APA taken singly or in combination because no motivation can be found for combining Iwamuro and APA. Claims 15-20 depend from claim 14 and thus distinguish over the cited references at least for the same reasons as claim 14.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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Attachments
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FIG. 2C
(PRIOR ART)

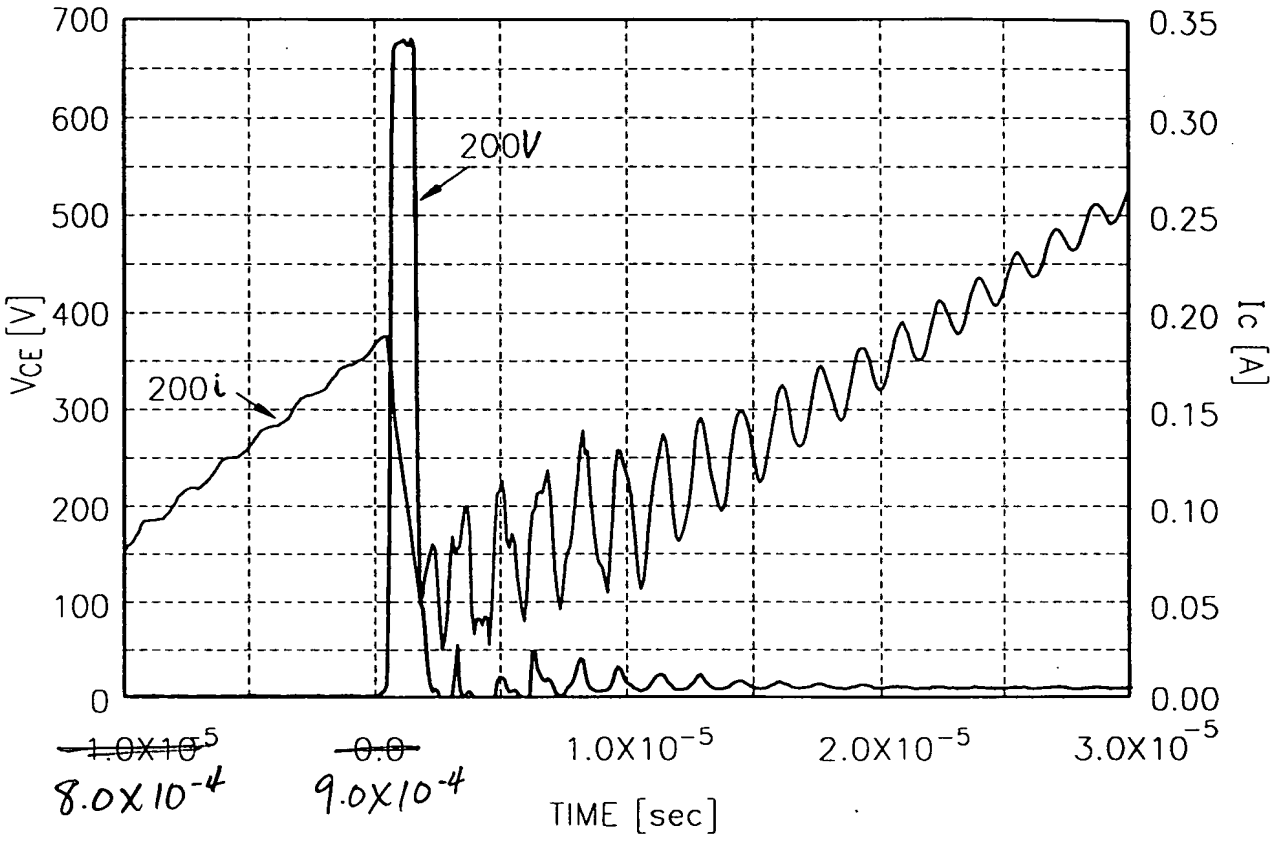

FIG. 4A

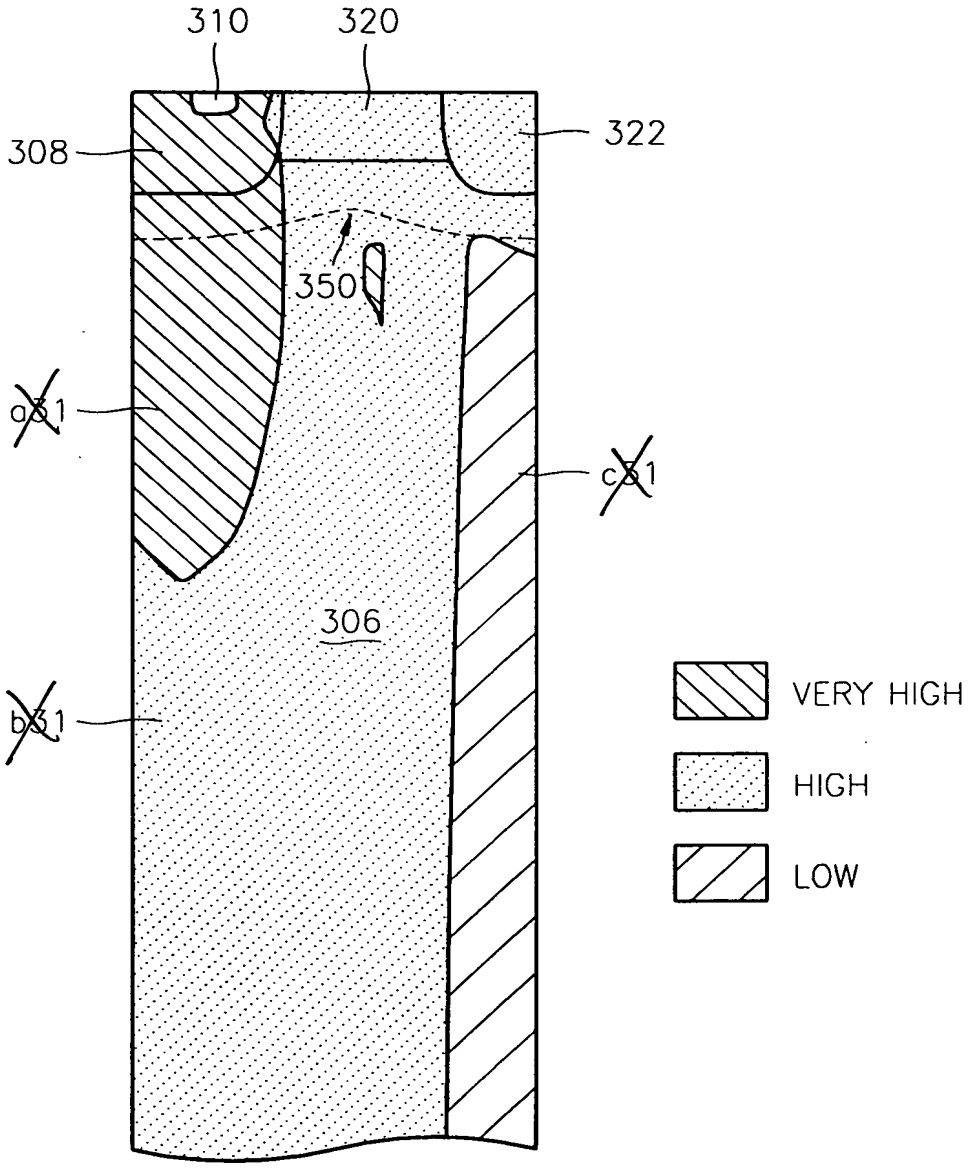

FIG. 4B

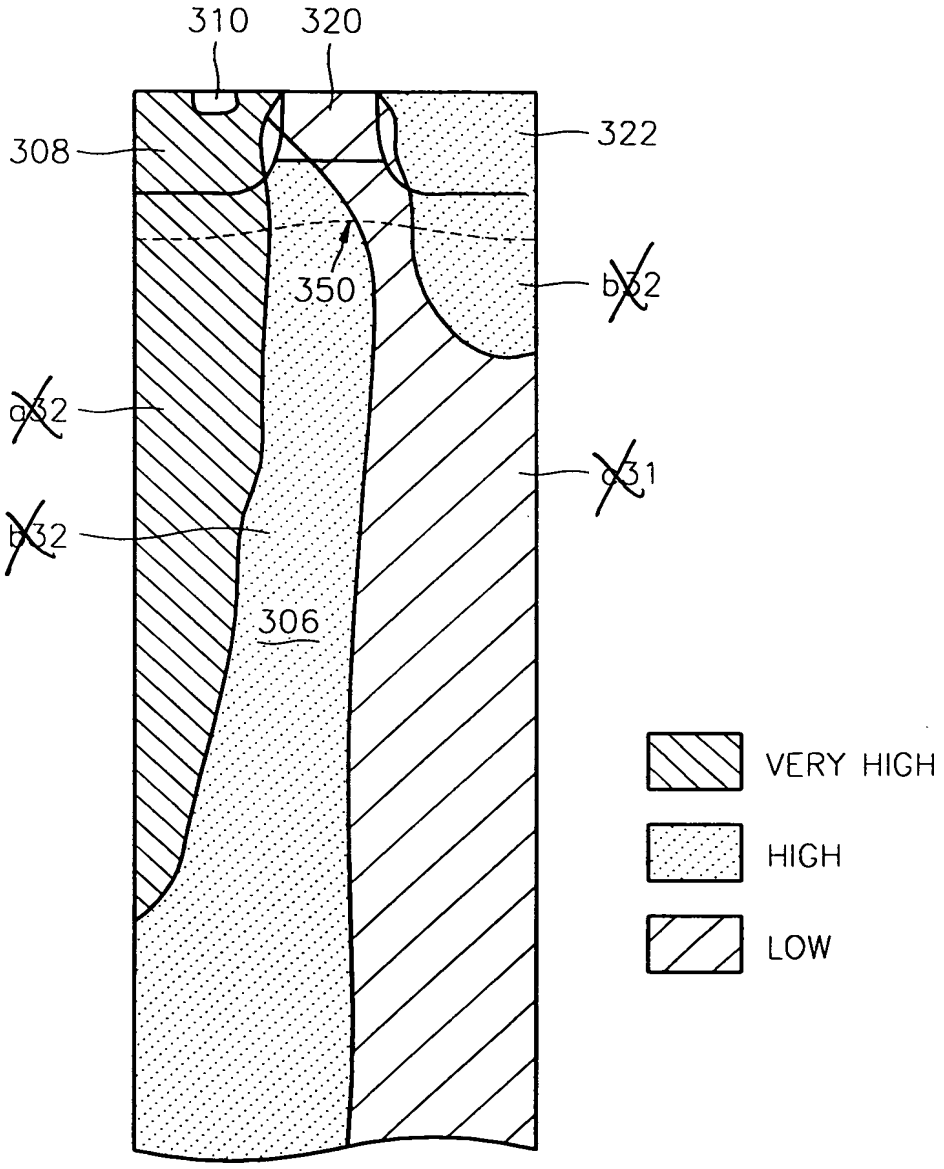

FIG. 4C